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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	PAPER NUMBER
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/29/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/646,535	ANDREEV ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

GUY LAMARRE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. Applicants' request for reconsideration filed on 10/13/2006 has been reviewed.

2. Amendment to the claims and specification filed of 10/13/2006 has been entered.

3. The drawings filed on 10/13/2006 have been accepted.

4. Applicants' arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1, 2, 3, 8, 9, 10, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roohparvar (US 5,825,782) in view of Fasang (US 4,433,413) and Neduva (US 5,612,916).

As per claim 1, Roohparvar teaches a system for allowing conventional memory test circuitry to test parallel memory arrays, comprising: bit pattern distribution circuitry that causes a probe bit pattern generated by said memory test circuitry to be written to each of said memory arrays; combinatorial logic, coupled to said pseudo-memory, that employs said portion and data-out patterns read from said memory arrays to generate a response bit pattern that matches said probe bit pattern only all of said data-out bit patterns match said probe bit pattern (fig. 4, 6, col. 5, lines 19-20, lines 31-58, col. 6, lines 30-39, col. 12, lines 33-45, col. 13, lines 19-38, Roohparvar).

However Roohparvar does not explicitly teach the specific use of a pseudo-memory, coupled to said bit pattern distribution circuitry that receives a portion of said probe bit pattern.

Fasang in an analogous art teaches that the decoder 140 has an output of "1" for any of the pseudo-memory addresses (col. 11, lines 21-23, Fasang). Fasang also teaches that the pseudo-memory address locations specified by the test program appears on the address lines of the system address bus 56 (col. 12, lines 35-37, Fasang). Fasang also teaches the parallel port test logic circuitry 44 (col. 16, line 31, Fasang). Fasang teaches that the pseudo-memory address decoder 140, which develops the P-MEM signal, may be constructed to use the outputs of the decoders 155...276 and provide a "1" output whenever any of those decoders has a "1" output (col. 19, lines 20-26, Fasang).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Roohparvar's patent with the teachings of Fasang by including an additional step of using a pseudo-memory, coupled to said bit pattern distribution circuitry, that receives a portion of said probe bit pattern.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a pseudo-memory, coupled to said bit pattern distribution circuitry, that receives a portion of said probe bit pattern would provide the opportunity to reduce the circuit and time required to test the parallel memory arrays.

Roohparvar also does not explicitly teach the specific use of causing said portion to bypass said memory arrays.

However Neduva in an analogous art teaches that the bit pattern, which is coupled through the array 20 bypassing the cells after being sensed by the sense amplifiers 22 is coupled to the compare circuit 27 through the lines 26 and then compared to the first pattern stored in the register 24 (fig. 2, col. 3, lines 38-42, Neduva).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Roohparvar's patent with the teachings of Neduva by including an additional step of causing said portion to bypass said memory arrays.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that causing said portion to bypass said memory arrays would provide the opportunity to increase speed of testing memory arrays.

- As per claim 2, Roohparvar, Fasang and Neduva teach the additional limitations.

Roohparvar teaches the system, wherein said bit pattern distribution circuitry comprises a multiplexer coupled to said each of said RAM arrays (col. 12, lines 65-67, Roohparvar).

- As per claim 3, Roohparvar, Fasang and Neduva teach the additional limitations.

Fasang teaches the system wherein portion is a single bit (col. 17, lines 53-55, Fasang).

- As per claim 8, Roohparvar, Fasang and Neduva the additional limitations.

Roohparvar teaches a method for allowing conventional memory test circuitry to test parallel memory arrays, comprising: causing a probe bit pattern generated by said memory test circuitry to be written to each of said memory arrays; and employing said portion and data-out bit patterns read from said memory arrays to generate a response bit pattern that matches said probe bit pattern only all of said data-out bit patterns match said probe bit pattern (fig. 4, 6, col. 5, lines 19-20, lines 31-58, col. 6, lines 30-39, col. 12, lines 33-45, col. 13, lines 19-38, Roohparvar).

Fasang teaches receiving a portion of said probe bit pattern into a pseudo- memory (col. 11, lines 21-23, col. 12, lines 35-37, col. 16, line 31, col. 19, lines 20-26, Fasang).

Neduva teaches causing said portion to bypass said memory arrays (fig. 2, col. 3, lines 38-42, Neduva).

- As per claim 9, Roohparvar, Fasang and Neduva teach the additional limitations.

Roohparvar teaches the method wherein said causing comprises sending a signal to a multiplexer coupled to said each of said RAM arrays (col. 12, lines 65-67, Roohparvar).

- As per claim 10, Roohparvar, Fasang and Neduva teach the additional limitations.

Fasang teaches the method wherein said portion is a single bit (col. 17, lines 53-55, Fasang).

- As per claim 15, Roohparvar, Fasang and Neduva teach the additional limitations.

Roohparvar teaches an integrated circuit, comprising: a processor; a plurality of identical memory arrays under control of said processor; conventional built-in test (BIST) circuitry; multiplexers, associated with said plurality of identical memory arrays and coupled to said processor and said conventional BIST

circuitry, that allows said conventional BIST circuitry to take said control from said processor (fig. 4, 6, col. 1, lines 24-32, col. 5, lines 19-20, col. 10, lines 8-10, lines 21-29, col. 12, lines 32-45, lines 65-67, Roohparvar); and a system that allows said conventional BIST circuitry to test said plurality of identical memory arrays in parallel, including: bit pattern distribution circuitry that causes a probe bit pattern generated by said conventional BIST circuitry to be written to each of said plurality of memory arrays, and combinatorial logic, coupled to said pseudo-memory, that employs said portion and data-out bit patterns read from said plurality of memory arrays to generate a response bit pattern that matches said probe bit pattern only if all of said data-out bit patterns match said probe bit pattern (fig. 4, 6, col. 5, lines 19-20, lines 31-58, col. 6, lines 30-39, col. 12, lines 33-45, col. 13, lines 19-38, Roohparvar).

Fasang teaches a pseudo-memory, coupled to said probe bit pattern distribution circuitry, that receives a portion of said probe bit pattern (col. 11, lines 21-23, col. 12, lines 35-37, col. 16, line 31, col. 19, lines 20-26, Fasang).

Neduva teaches causing said portion to bypass said memory arrays (fig. 2, col. 3, lines 38-42, Neduva).

- As per claim 16, Roohparvar, Fasang and Neduva teach the additional limitations.

Fasang teaches the integrated circuit wherein said portion is a single bit (col. 17, lines 53-55, Fasang).

8. Claims 4, 5, 6, 7, 11, 12, 13, 14, 17, 18, 19, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roohparvar (US 5,825,782), Fasang (US 4,433,413) and Neduva (US 5,612,916) as applied to claim 1, 8, 15 above, and further in view of Connor et al. (US 5,553,082).

As per claim 4, Roohparvar, Fasang and Neduva substantially teach the claimed invention described in claim 1 (as rejected above).

However Roohparvar, Fasang and Neduva do not explicitly teach the specific use of the system, wherein said combinatorial logic comprises comparator circuitry that produces a zero bit only if all of said data-out bit patterns match said probe bit pattern.

Connor et al. in an analogous art teach that the marching pattern causes all XNOR gates to match except the one gate which has a "1" on port B. This causes the final output of the comparator 40 to exhibit a "0" value (col. 6, lines 1-3, Connor et al.). The examiner would like to point out that the comparator could also produce a "0" bit when the pattern matches.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Roohparvar's patent with the teachings of Connor et al. by including an additional step of using the system, wherein said combinatorial logic comprises comparator circuitry that produces a zero bit only if all of said data-out bit patterns match said probe bit pattern.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the system, wherein said combinatorial logic comprises comparator circuitry that produces a zero bit only if all of said data-out bit patterns match said probe bit pattern would provide the opportunity to determine memory fault by analyzing the final output of the comparator.

- As per claim 5, Roohparvar, Fasang, Neduva and Connor et al. teach the additional limitations. Connor et al. teach the system, wherein said combinatorial logic further comprises corrector circuitry that produces said response bit pattern that matches said probe bit pattern only if said comparator circuitry produces said zero bit (col. 6, lines 4-10, Connor et al.).

- As per claim 6, Roohparvar, Fasang, Neduva and Connor et al. teach the additional limitations. Connor et al. teach the system, wherein said response bit pattern differs from said probe bit pattern by a single bit if at least one of said data-out bit patterns fails to match said probe bit pattern (col. 5, line 67 to col. 6, line 4, Connor et al.).

- As per claim 7, Roohparvar, Fasang, Neduva and Connor et al. teach the additional limitations. Connor et al. teach the system wherein a portion of said response bit pattern matches a corresponding portion of a data-out bit pattern from one of said memory arrays (col. 6, lines 1-2, Connor et al.).

- As per claim 11, Roohparvar, Fasang, Neduva and Connor et al. teach the additional limitations. Connor et al. teach the method wherein said employing comprises producing a zero bit only if all of said data-out bit patterns match said probe bit pattern (col. 6, lines 1-3, Connor et al.). The examiner would like to point out that the comparator could also produce a "0" bit when the pattern matches.

- As per claim 12, Roohparvar, Fasang, Neduva and Connor et al. teach the additional limitations.

Connor et al. teach the method wherein said employing further comprises producing said response bit pattern that matches said probe bit pattern only if said zero bit is produced (col. 6, lines 4-10, Connor et al.).

- As per claim 13, Roohparvar, Fasang, Neduva and Connor et al. teach the additional limitations. Connor et al. teach the method wherein said response bit pattern differs from said probe bit pattern by a single bit if at least one of said data-out bit patterns fails to match said probe bit pattern (col. 5, line 67 to col. 6, line 4, Connor et al.).

- As per claim 14, Roohparvar, Fasang, Neduva and Connor et al. teach the additional limitations. Connor et al. teach the method wherein a portion of said response bit pattern matches a corresponding portion of a data-out bit pattern from one of said memory arrays (col. 6, lines 1-2, Connor et al.).

- As per claim 17, Roohparvar, Fasang, Neduva and Connor et al. teach the additional limitations. Connor et al. teach the integrated circuit wherein said combinatorial logic comprises comparator circuitry that produces a zero bit only if all of said data-out bit patterns match said probe bit pattern (col. 6, lines 1-3, Connor et al.). The examiner would like to point out that the comparator could also produce a "0" bit when the pattern matches.

- As per claim 18, Roohparvar, Fasang, Neduva and Connor et al. teach the additional limitations. Connor et al. teach the integrated circuit wherein said combinatorial logic further comprises corrector circuitry that produces said response bit pattern that matches said probe bit pattern only if said comparator circuitry produces said zero bit (col. 6, lines 4-10, Connor et al.).

- As per claim 19, Roohparvar, Fasang, Neduva and Connor et al. teach the additional limitations. Connor et al. teach the integrated circuit wherein said response bit pattern differs from said probe bit pattern by a single bit if at least one of said data-out bit patterns fails to match said probe bit pattern (col. 5, line 67 to col. 6, line 4, Connor et al.).

- As per claim 20, Roohparvar, Fasang, Neduva and Connor et al. teach the additional limitations. Connor et al. teach the integrated circuit wherein a portion of said response bit pattern matches a corresponding portion of a data-out bit pattern from one of said memory arrays (col. 6, lines 1-2, Connor et al.).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dipakkumar Gandhi
Patent Examiner